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PROCESS FOR PLANARIZING ARRAY TOP OXIDE IN VERTICAL MOSFET DRAM ARRAYS

Abstract

The present invention provides a process for planarizing array top oxide (ATO) in vertical MOSFET DRAM arrays. In contrast to the prior art ARC-RIE planarization method for EA/ES (etch array/etch support) module, the present invention takes advantage of chemical mechanical polishing (CMP) technique to overcome residue problems that used to occur at the transition region or array edge. It might cause capacitor device failure when ATO residue is left on the transition region.